New Space Communications Capabilities Available for NASA's Discovery and New Frontier Programs

January 5, 2006

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1.0 INTRODUCTION

NASA's Deep Space Network Technology Program, funded primarily by NASA's Science Mission Directorate (SMD), is developing technologies needed for realizing the future evolutionary systems in the NASA Strategic Plan. That plan is guided by four basic principles; reliably achieving negotiated mission goals, increasing the science data return of future missions 1000X by 2015, providing standard and cost effective mission interfaces, and growing an evolving infrastructural architecture for seamless communications and navigation across the solar system. The plan contains a number of strategic goals that pertain to both spacecraft and ground systems. While both of these are important for achieving end-end system performance improvements, the spacecraft technologies are more directly applicable to specific missions and are frequently candidates for in-space validation. It is the purpose of this roadmap document to describe the spacecraft technologies available for future Discovery and New Frontiers mission planners to encourage infusion of these technologies, if not on an operational standpoint, at least for in-flight technology validations.

Section 2 of this document contains descriptions of key NASA spacecraft technology developments. Each technology description consists of relevant background material, specific descriptions of the technology, and a timeline showing the key planned milestones during the technology development. Reference and further reading material for each of the listed technologies are given in Section 3.

After each technology description, a POC is provided. Acquisition and costs should be discussed directly with these POCs.

2.0 KEY TECHNOLOGY DESCRIPTIONS

2.1 LDPC FLIGHT ENCODERS

2.1.1 DESCRIPTION

New Frontier and Discovery class missions will require very efficient communication systems, capable of supporting high data rates in the 10 to 100 Mbps range within stringent spectral constraints. Low Density Parity Check (LDPC) codes are high-speed error-correcting codes for large data rates. The currently available Turbo decoders would require an unwieldy amount of hardware to achieve these rates. LDPC codes enable efficient communication at data rates 10 Mbps and beyond because their coding gains are comparable to turbo codes and their encoders and decoders can be implemented using parallel-processing architectures, enabling significant speed improvements.

The NASA Deep Space Network (DSN) has implemented Turbo decoders necessary to support Messenger, Stereo, MRO, and other upcoming missions that require maximum communications channel power efficiency at data rates up to 1.6 Mbps. Starting from 2007 new missions, and in particular New Frontier and Discovery missions, are expected to require data rates from 10 to 100 Mbps.

The NASA Technology Program is producing a modular FPGA implementation for the encoder for all coding overhead rates and block sizes in the code family recently developed and submitted for CCSDS standardization. The encoder design is re-usable by multiple missions, and the FPGA-based encoder module can be easily infused into flight projects. Prototype software encoders are also available to flight projects that require only modest data rates where the encoding can be achieved in mission on-board microprocessor.

LDPC encoders have recently been implemented on FPGA's with two different architectures: Universal - - for any LDPC code (useful for research and some potential CCSDS standardization outcomes); and Quasi-cyclic codes - - where code parameters are more specialized and less logic (smaller FPGA) is required. Prototypes are available for a 100 Msps universal LDPC encoder, and for a specialized 100 Msps block-circulant LDPC encoder with lower complexity.

LDPC encoders work by performing a sequence of (mostly) sparse matrix operations. Fast encoders can be obtained by representing circulants with polynomials, by using simple convolution to perform polynomial multiplication, and by inverting a set of small matrices using abstract algebra. These encoders can be implemented by using popular FPGAs (e.g., Xilinx Virtex-II XC2V8000-4), and they can also reside in COTS rad-hard devices (e.g., Virtex-II XC2V6000). These encoders can be reconfigured in flight for different codes.

Alternative encoder architectures are based on *iterative* encoding which essentially use a simple decoder to correct erasures and hence compute the parity. This method has the potential for even higher speeds than quasi-cyclic or block-circulant designs. FY06 development plans include the implementation of a fully tested (up to) 100 Mbps encoder, complete I/O interfaces and ready for flight infusion. A goal for FY07 is the design of a mapper to interface the encoder output to the input of a bandwidth efficient modulator for use in highly spectral constrained applications. This would be tested and available for infusion in FY08. See Section 3.1 for further reading and references.

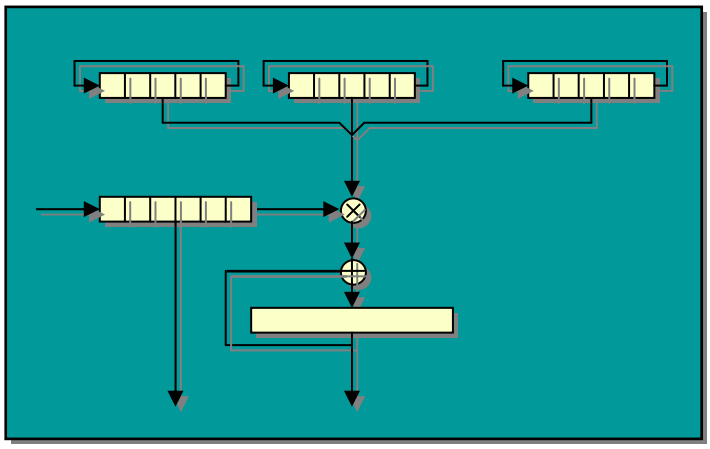

Figure F-1. Universal Encoder Design for Family of LDPC Codes

2.1.2 SCHEDULE

- FY06: Implement 100 Mbps FPGA encoder; Rad-hard FPGA encoder
- FY07: Encoder mapper for bandwidth efficient modulator
- FY08: Implement encoder and mapper ready for flight validation

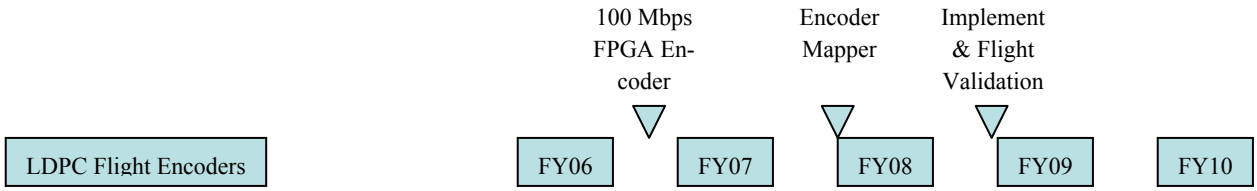

Figure F-2. LDPC Flight Encoder Schedule

2.1.3 POC

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2.2 KA-BAND TRAVELING WAVE TUBE AMPLIFIER (TWTA)

2.2.1 DESCRIPTION

Higher data rate communications requires higher Effective Isotropic Radiated Power (EIRP) in order to maintain the necessary link signal-to-noise ratio. Greater EIRP in turn requires either larger antenna apertures, higher RF frequencies, and/or more amplifier power. Larger increases in data transmission are not practical within the constraints of the X-band deep space downlink allocation, so utilization of Ka-band is used with its ten times greater allocation. Current Ka-band TWTA state-of-the-art is the 35 W unit that is being experimentally validated on board MRO, presently in transit to Mars.

NASA is currently mid-way through development program to produce and flight qualify a 180 W Ka-band EQM TWTA by the end of 2006. This will advance the hardware to TRL6. The unit is based upon the 180 W Ka-band TWT (vacuum tube) produced by the Jupiter Icy Moon Orbiter (JIMO) technology development program through a contract monitored by NASA Glenn Research Center. The current program is developing the required high voltage power supply (HVPS) needed for a complete TWTA and also includes integration and qualification testing. The HVPS has completed breadboard testing, and the EQM HVPS has started fabrication. The two figures below show the 180 W TWT and the breadboard HVPS

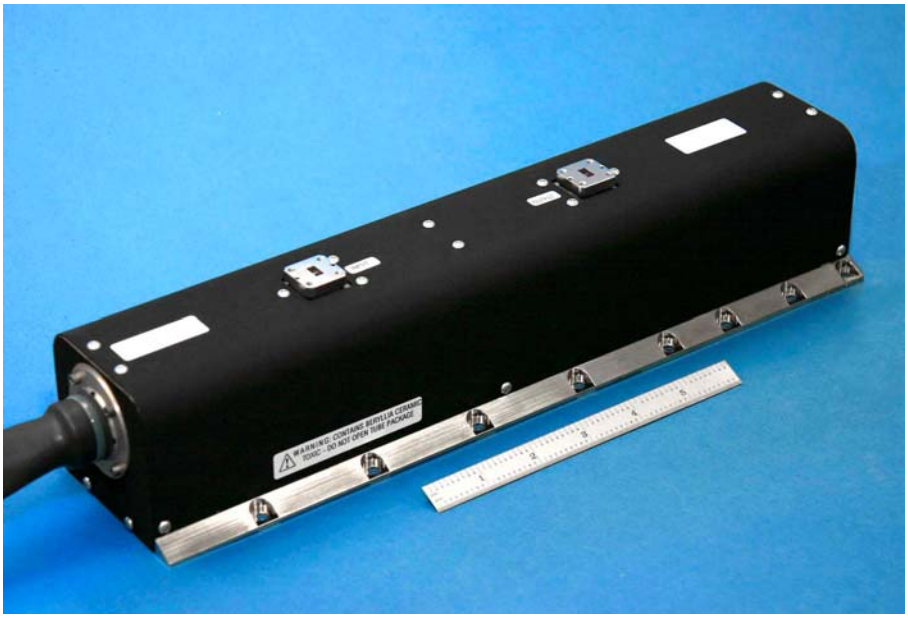

Figure F-3. 180 W Ka-Band TWT

When completed this new TWTA will provide a nominal 7.1 dB downlink data return improvement over the present 35W Ka-band TWTA. The TWT design is very versatile; it can be scaled to any power level from 180 W down to as low as 35 W. Potential customers for this power range include the Mars program, the Discovery and New Frontier missions, and other deep space or near earth programs requiring Ka-band transmit powers between 35 and 180 watts output. In fact, the Kepler project is already planning touse a 35 W version of this TWTA. To obtain even higher power levels, further work will be needed but test data on the current hardware indicates that the existing design can probably be scaled up to 250 W RF output with only a modest development program. See Section 3.2 for further reading and references.

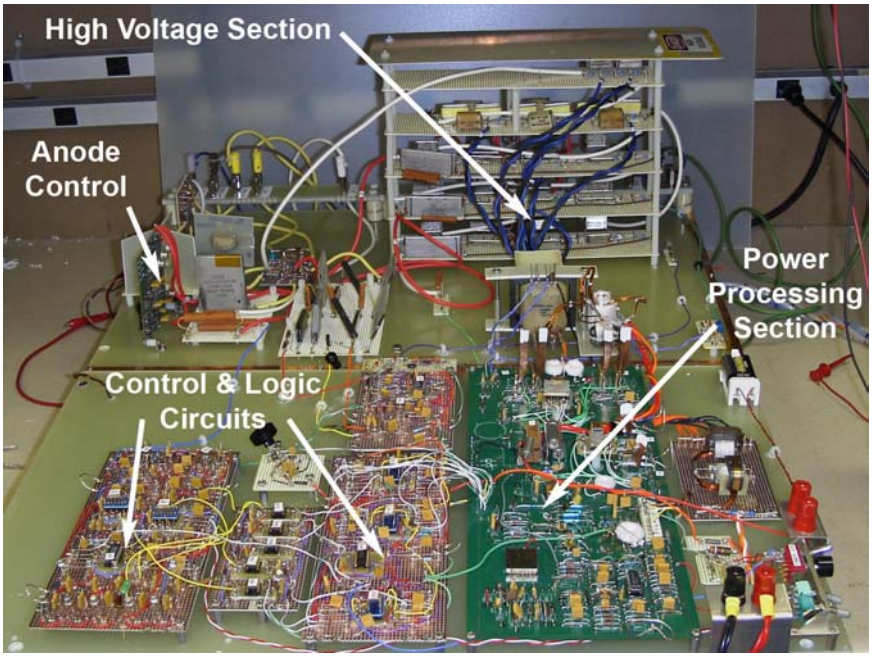

Figure F-4. Breadboard HVPS for 180 W TWTA

2.2.2 SCHEDULE

- FY06 Integrate TWT and HVPS
- Flight qualify 180 W TWTA
- FY07 Delivery and verification tests at JPL
- FY07 Available for flight validation and infusion – (TRL 6)

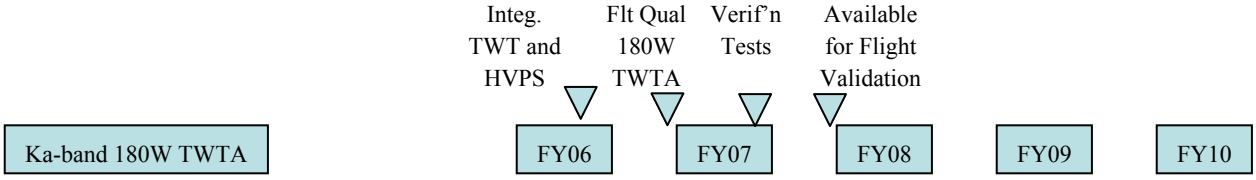

Figure F-5. TWTA Schedule

2.2.3 POC

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2.3 UPLINK CODING

2.3.1 DESCRIPTION

The current uplink coding system is simple and reliable, but emphasizes reliable detection and removal of any occasionally received incorrect transmissions rather than ensuring that the uplink signals are received correctly in the first place. Advances in coding technology can allow much more power efficient utilization of the uplink communications channel while simultaneously ensuring that transmission errors are not accepted. This is crucial for future missions that require higher data rate uplinks (e.g. for program uploads) than the 2 kbps uplinks used by current missions.

Current uplink coding fails to provide any appreciable coding gain. It uses a short-block (63,56) BCH code that achieves 1.1 dB of coding gain in Single Error Correction (SEC) mode, but a 0.6 dB loss in Triple Error Detection (TED) mode and limits the information that can be sent to spacecraft in an emergency. It was designed only for routine command applications, is now becoming operationally inefficient and obsolete. Mission requirements for the uplink vary depending on phase of mission and criticality of data. A full uplink coding solution must include enough error detection capability to achieve extremely low undetected error rates. An additional constraint is compatibility with variable length frames. The CCSDS Telecommand (TC) uplink protocol and the Proximity-1 link protocol both utilize variable length frames, which are incompatible with current uplink forward error correction coding methods. Different uplink applications have different requirements and may require different coding solutions. There are at least three application profiles distinguished by required data rates:

Type A - Emergency uplink: 8 bps; ~100 bits long messages, very sporadic usage
Type B - Routine command (B-1) and ARQ (Automatic Repeat Query) acknowledgments (B-2): 1 to 4 Kbps; several ~100 bits long messages (Current coding systems were designed for Type B.)
Type C - File uploading: 4 to 1000 Kbps (e.g., operating system program uploads)

There is an increasing need to extend uplink service to Types A and C in addition to Type B for which the current system was designed.

NASA is funding technology investments of possible coding solutions and their applicability to each of the different uplink applications. The end result will be the design and selection of an appropriate set of codes for each scenario, along with a strategy for using uplink coding and a description of the benefits of each coding solution. These include no coding, the current BCH code, (3,1/2) and (7,1/2) convolutional codes, and a suitable *family* of state-of-the-art LDPC codes for the scenarios. Suitable LDPC code block sizes range from around 100 bits for Type A to around 1024 bits for Type B, to around 16K bits for Type C. This work also investigates the use of ARQ on the uplink. Coding solutions developed for downlink and in-situ applications may be adaptable to (some of) the uplink scenarios. This would promote compatibility of encoder/decoder hardware and reduce overall system costs.

For Type C, in which the data rates are significantly higher than the data rates for which the original uplink code was designed, the expected coding gain at a bit error rate of 10^{-6} is about 9.7 dB. Realizing these coding gains only requires an onboard FPGA LDPC decoder together with receiver improvements that produce uplink channel symbol confidence values and allow for synchronize at low-SNR levels. By selecting an uplink code family that is compatible with that already selected for in-situ downlink applications, the same onboard decoder could be used for both types of applications. These LDPC code applications require a separate error detection

(CRC) code to guarantee low undetected error rates. See Section 3.3 for further reading and references.

2.3.2 SCHEDULE

- FY06: Analysis of four uplink scenarios, design of LDPC code families, comparative performance analysis, and selection of most appropriate coding solution for each scenario (Q4)
- FY07: FPGA implementations of the selected onboard uplink decoders
- FY08: Flight implementation and validation

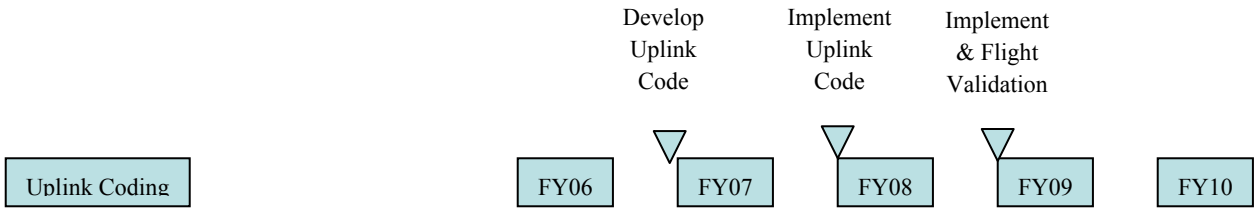

Figure F-6. Uplink Coding Schedule

2.3.3 POC

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2.4 ANTENNA/STRUCTURES MODELING TOOLS

2.4.1 DESCRIPTION

The Technology Program is developing an Antenna/Structures Electro-Magnetic (EM) Modeling Tool that reduces the time required to model and evaluate the impacts of local mounting environments of spacecraft antennas on the resulting RF antenna beam profiles by at least an order of magnitude. The tool will benefit all Deep Space programs, including those that employ in-situ assets such as landers, rovers and fixed platforms. The tool is a full-wave Computational EM modeling (CEM) tool capable of accurately simulating the true RF environment of an entire antenna/vehicle/platform based on inputs from standard CAD model files. Simulation products include antenna gain in the presence of multi-path and on-board RF field intensities for controlling EMI levels.

Current antenna modeling tools for predicting full-wave EM environments are confined to limited size metallic structures and lower-frequencies (UHF). Computations on larger, multi-material structures, or on smaller structures at higher frequencies, are too computationally intensive to be practical. As a result, only small portions of the antenna/spacecraft/platform environment can currently be modeled at any one time and the computation time is on the order of days for all the pieces. This piecemeal view of the RF environment is not representative of the true multi-path environment, especially at UHF. There is currently a dependence on using full scale mockups and testing to estimate many of these RF characteristics. Unfortunately, as with any experimental approach, the accuracy of the measurements as well as the fidelity of the mockup are always in question.

The modeling tool being developed will enable projects to quickly (within a day or less) select antenna types and locations for in-situ antennas to minimize multi-path and EMI using accurate simulations of the complete spacecraft/vehicle/platform, without costly mockup iterations. Also, in the event that multi-path issues do show up unexpectedly post-launch, the tool will allow projects to be able to obtain accurate estimates of the "in-flight" configuration that could guide post-launch re-planning to optimize in-situ telecom link closure.

The tool will provide end-to-end capability for taking full spacecraft/vehicle configurations from a standard CAD file and producing accurate, full-fidelity predictions of the RF environment, including multi-path and near-field EMI, for frequencies up to and including S-band. The EM tool development goals are to increase the size of the computational models (spacecraft/vehicle/platform) by ~10X and the overall computing speed by ~100X. See Section 3.4 for further reading and references.

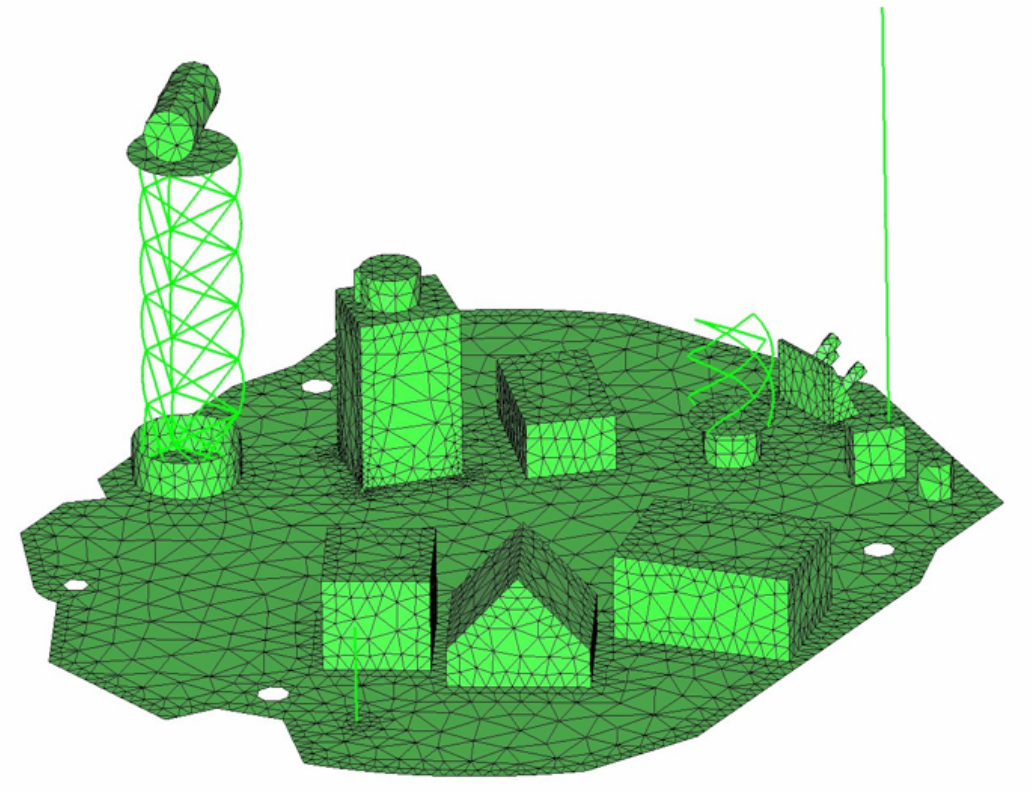

Figure F-7. Example: In-Situ Antenna, Phoenix Deck Mesh Model

2.4.2 SCHEDULE

- FY06 Develop and test Conjugate Gradient Solver
- FY07 Test CEM Tool and conduct trials with candidate spacecraft
- FY08 Complete updating and release CEM Tool

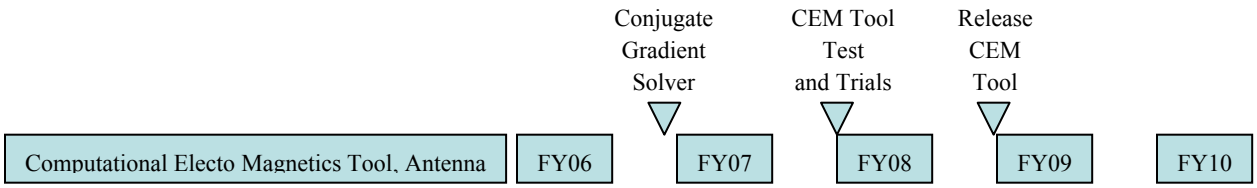

Figure F-8. CEM Schedule

2.4.3 POC

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2.5 DATA COMPRESSION

2.5.1 DESCRIPTION

Progressive Wavelet Image Compression (ICER)
The ICER image compressor provides image reconstruction when up to 90% of the original image file size has been eliminated before transmission. Much more of the example image in Figure F-9 would be lost using the common JPEG compressor data recovery techniques. For many missions, images comprise the large majority of the data transmitted. Failing to use a state-of-the-art image compressor reduces the number of images that can be transmitted over a given communications channel.

ICER is an image compressor that is being used in software by the Mars Exploration Rovers for compression of a large majority of the image data returned. ICER delivers state-of-the-art compression effectiveness, allowing the MER rovers to return more image data than would be possible using the JPEG compressor used by Mars Pathfinder. ICER can be used to provide lossless or lossy compression. It incorporates an effective error-containment technique, and a new flexible method of controlling the tradeoff between image quality and compressed data volume.

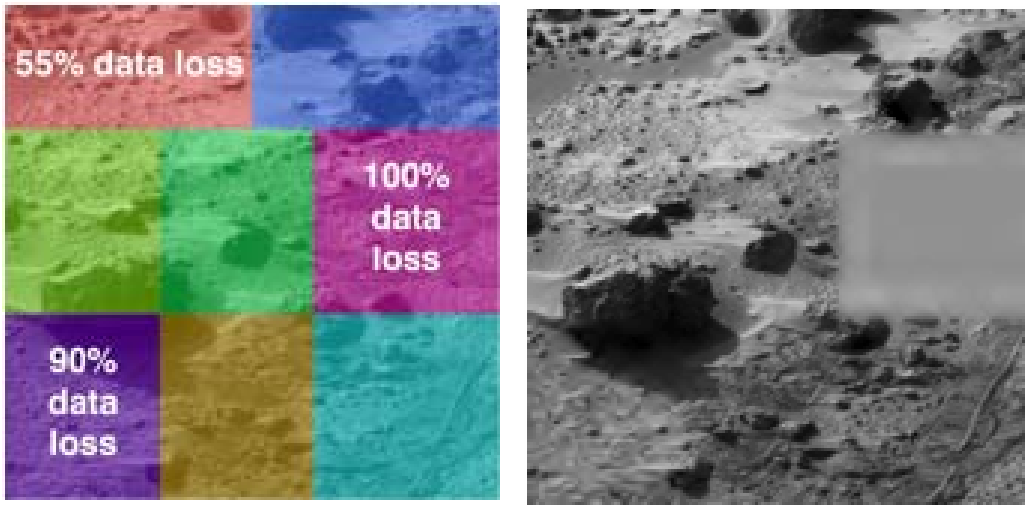

Figure F-9. Example: Original and reconstructed image using ICER after data loss

ICER is flight-proven and ready for infusion. ICER is a general-purpose image compressor that is widely applicable to missions with imaging instruments that are capable of performing compression in software.

Hyper-spectral Data Compression (general)
Hyper-spectral imaging instruments are capable of producing enormous volumes of data that quickly overwhelm the deep space downlink and require massive onboard storage capabilities. Effective techniques for compressing such data sets are essential to overcome downlink limitations and make more efficient use of onboard storage. The traditional approach to hyper-spectral data compression is to apply existing two-dimensional image compressors to each spectral band independently. A more effective way to compress such image data sets is to use new compres-

sors that effectively exploit correlations in all three dimensions (two spatial and one spectral) to improve compression performance.

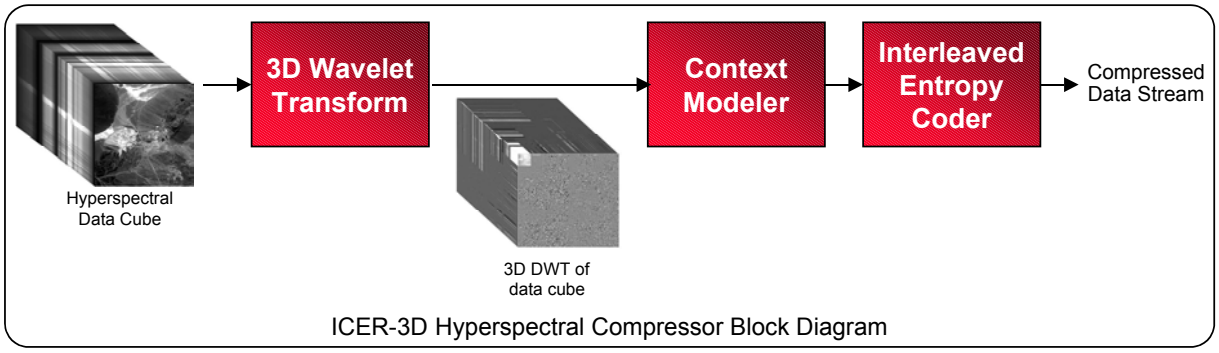

Figure F-10. ICER-3D Hyper-spectral Compressor Block Diagram

ICER-3D

ICER-3D is an extension of the ICER compressor to hyper-spectral data sets. ICER-3D uses a 3-D wavelet decomposition to produce de-correlation in the spectral dimension as well as both spatial dimensions.

ICER-3D inherits much of its design, and hence some of its desirable features, from ICER. ICER-3D compression is *progressive*, which means that compressed information is organized so that as more of the compressed data stream is received, reconstructions with successively higher overall image quality can be reproduced. A bit stream with this property is often referred to as *embedded*. Since ICER-3D uses reversible wavelet transforms, it can provide lossless or lossy compression. Hence, it can efficiently meet the needs of missions requiring both types of compression. Truncating an embedded data stream by increasing amounts produces a graceful degradation in the reconstructed image quality.

ICER-3D also incorporates an effective error-containment technique to limit the effects of data loss during transmission. Because compression is progressive within each error-containment segment, when data loss does occur, any received data for the affected segment that precedes the lost portion will allow a lower fidelity reconstruction of that segment.

ICER-3D FPGA Hardware Implementation

ICER-3D has been implemented in FPGA hardware. The implementation employs state-of-art FPGAs, such as Xilinx Virtex II and Virtex II Pro. The implementation is based on a recently developed efficient parallel implementation of the discrete wavelet transform on an FPGA. The wavelet transform module is line-based, which means that the wavelet transform is computed as the lines of image data arrive, rather than waiting for an entire frame of data. This accommodates push-broom sensors and reduces memory requirements, which can be an enabling feature for very large data sets.

The hardware design is high performance, fully parallel, low-power and scalable. It provides lossless compression at a data rate of 4.5 Msamples/sec (for a single module) at a conservative clock speed of 50MHz. Modules can be combined in parallel and/or run at higher clock rates for increased speed. The design uses less than 6.5 Watts of power per module.

Fast Lossless Hyper-spectral Compressor

Also developed is a highly effective low-complexity lossless compressor suitable for multi-spectral or hyper-spectral images. The fast lossless compressor has modest computational and memory requirements and is suitable for hardware or software implementation.

The algorithm applies predictive techniques to de-correlate hyper-spectral image data based on a context model derived from the values of nearby data elements. This allows data to be processed sequentially in the order read from the instrument sensors (analogous to raster-scan processing in two-dimensional lossless image compression). Sequential processing facilitates fast compression, and since data re-ordering is not necessary, it significantly reduces memory demands compared to transform-based techniques, which require buffering of a significant number of data samples before the transform can be computed. The predictive approach generates a sequence of residuals with low entropy (uncertainty) , and associated probability estimates, and encodes the residual sequence using an entropy coding scheme. Compared to the wavelet-based method, this lossless compression approach provides faster compression with lower onboard memory demands. And, because it is specially designed for lossless (only) compression, its lossless compression performance is even better than that obtained by ICER-3D. The compressor is robust; it requires no training data or other specific information about the nature of the spectral bands. The compressor is easily configurable for parallel processing and is well suited to push-broom instruments.

On AVIRIS hyper-spectral test data, this fast lossless compressor noticeably outperformed the multi-spectral compression mode of the USES/Rice lossless compressor. For a fixed constraint on downlink data volume, a mission could return 40% more data using this compressor than with the USES multi-spectral compressor.

The compressor has been implemented in prototype C software. A flight software implementation and documentation would require about 1 year. FPGA hardware implementation to TRL6 would require about 2 years. See Section 3.5 for further reading and references.

2.5.2 SCHEDULE

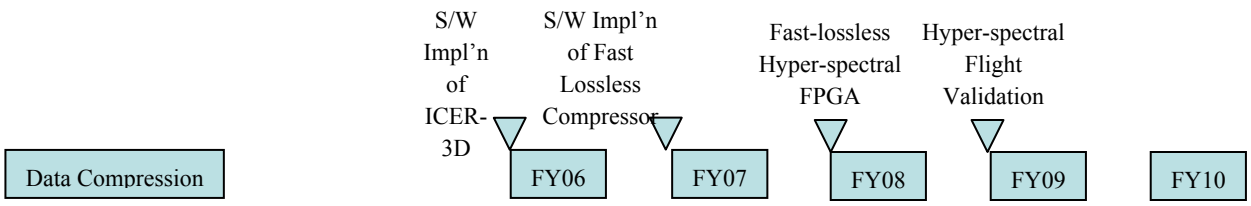

Figure F-11. Data Compressor Schedule

2.5.3 POC

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2.6 ONBOARD EVENT DETECTION & RESPONSE

2.6.1 DESCRIPTION

The typical response sequence to an event observed by remote spacecraft is to capture data that happens to contain the event, downlink the data to Earth, decide (usually people) on an appropriate response, and uplink a command for subsequent observations. With human operator decision-making in the loop for events occurring at the outer planets, the response time could be many hours. *Onboard Event Detection and Response* technology enables a spacecraft or rover to autonomously recognize dynamic science events and to use these detections for content-based data compression and/or to enable a coordinated onboard response within minutes. This new technology results in the ability to collect data at the rate of the instruments and the spacecraft capabilities, rather than constraining data collection based on downlink bandwidth long-loop decision processes. This will allow ongoing monitoring of phenomena, increasing the chances for observing rare and dynamic events as well as ensuring data with the highest science value is collected for subsequent transmission to Earth.

The Onboard Autonomous Science Investigation System (OASIS) has demonstrated limited opportunistic science during a rover traverse using field test rovers. Circumventing technical limitations on event detection and response time enables several classes of science investigations and missions that would be impractical with the long latencies and limited bandwidth of the typical "sense-downlink-decide-uplink" command cycle:

- Scan for rare or infrequent events, such as a Martian dust devil, and alert the science team when they are found. Such scans are impractical without onboard science event detection because there is insufficient bandwidth to downlink all the images and insufficient workforce to search through them. Faster recognizers will ensure that these events are captured and downlinked.

- Quick response to an episodic event, such as a comet out-gassing or dust storm, by taking follow-up images at a higher resolution or with other sensors. Fast responses are necessary to capture short-lived events and the critical science at the early stages of the event.

- Respond to dynamic events such as Europan ice motion, dust devils, tsunamis and storms. Existing static-event detectors cannot accurately recognize these phenomena.

- Coordinate observations of events by alerting other assets (orbiter or rover) to take follow-up images. Absolute localization (rather than relative to the image frame) is needed to accurately target the event for tasking other assets or taking a follow-up image before moving out of view.

Candidate missions for this technology include Europa and other Jovian system orbiters, Titan aerobots, Venus landers and orbiters, Mars surface, orbital, and aerial missions, and comet missions among others. See Section 3.6 for further reading and references.

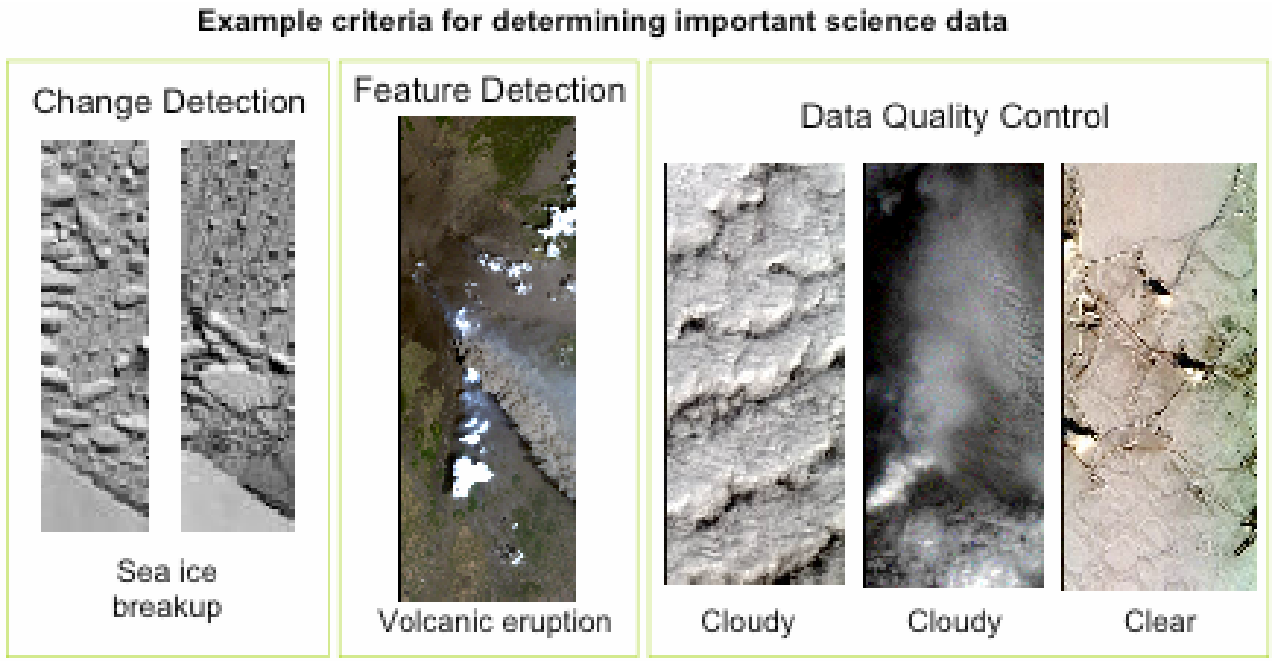
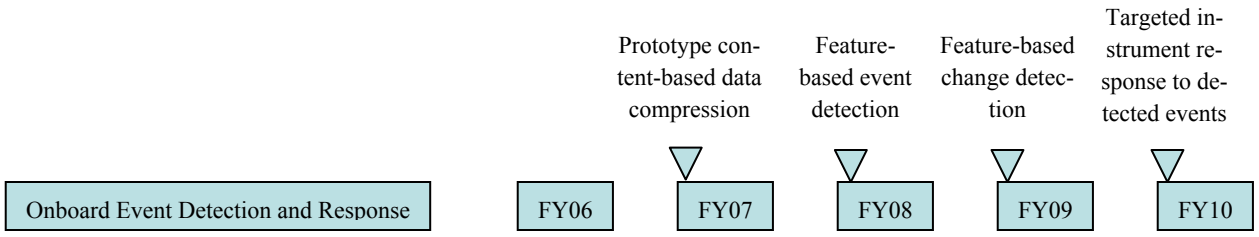


Figure F-12. Example Criteria for Determining Important Science Data

2.6.2 SCHEDULE



2.6.3 POC

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2.7 HIGH SPEED DATA HANDLING SUBSYSTEM

2.7.1 DESCRIPTION

Current space communications protocol implementations use the spacecraft central Command and Data Handling (C&DH) computer to retrieve data from mass storage devices, format that data into the proper protocol units, and feed the resulting data stream to a telecom transceiver. As protocols become more complex with the addition of features such as file management and automated reliability, this process becomes slower and more inefficient. A new High Speed Data Handling (HSDH) Subsystem has been developed whereby complex telemetry processing functions can be removed from the C&DH processor, and hosted in a space-qualified FPGA. This accomplishes both a major reduction in C&DH processing power required for telemetry, as well as providing high-speed technology for CCSDS File Delivery Protocol (CFDP) and link layer protocols used in high-speed telemetry applications.

Current spacecraft such as Deep Impact have shown that significant amounts of C&DH processor time are taken up with the communication protocol operations. Laboratory tests have also shown that with a state-of-the art IBM Power PC (PPC) 750 computer that is available for spacecraft C&DH systems, data throughput rates are limited to a few megabits per second and use most of the available processor resources. Current flight hardware and software implementations will not accommodate the high data rates required for many future missions, which range from 20 Mbps to well over 100 Mbps.

The breakthrough HSDH Subsystem implementation uses an FPGA with an on-board PPC co-processor. While other simpler link-layer telecommunications protocols have been ported to FPGA's before, this is the first instance where the complex CFDP has been hosted in an advanced FPGA with an on-board PPC co-processor. This implementation has already demonstrated 100 to 200 Mpbs throughput using reliable-mode CCSDS protocols. The laboratory implementation currently includes interfaces to mass storage, legacy radios and newer software-defined radios such as ELECTRA.

Figure F-13 shows a candidate configuration for a spacecraft with both an ELECTRA UHF radio for proximity communications and a Small Deep Space Transponder (SDST) for Deep Space communications.

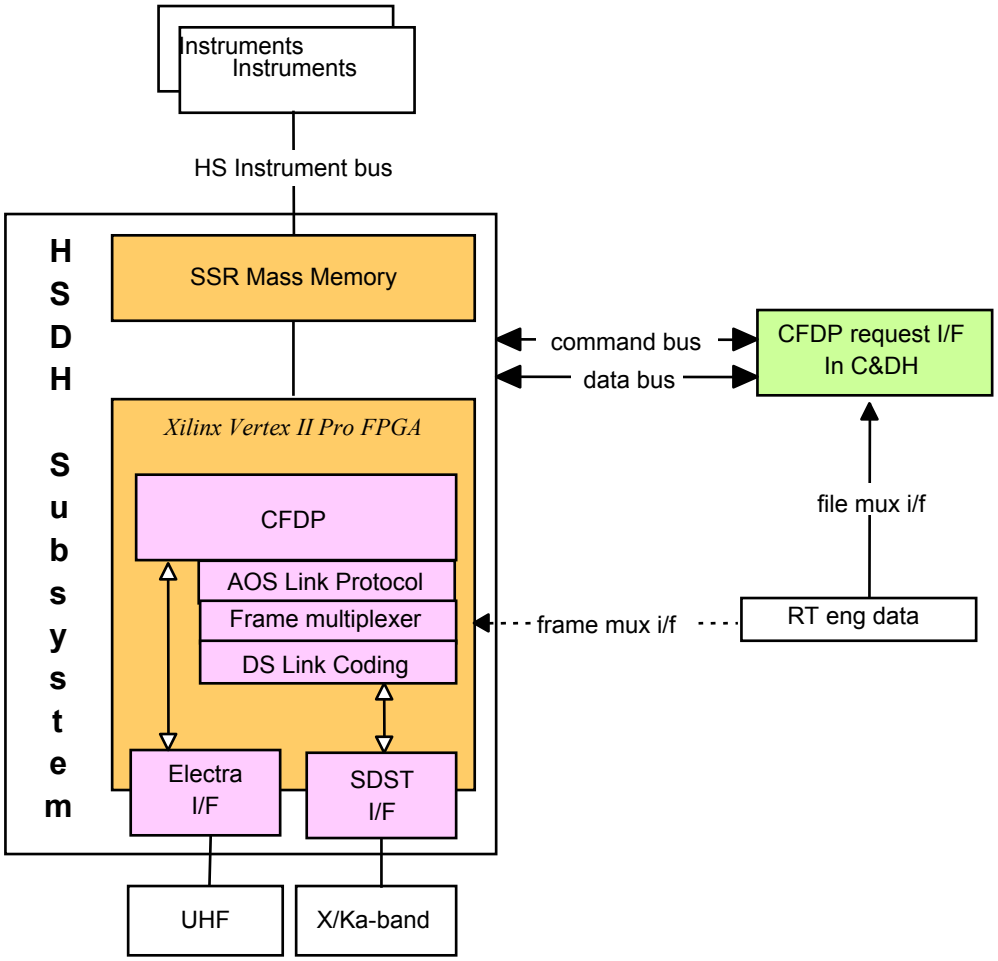


Figure F-13. HSDH Subsystem candidate configuration

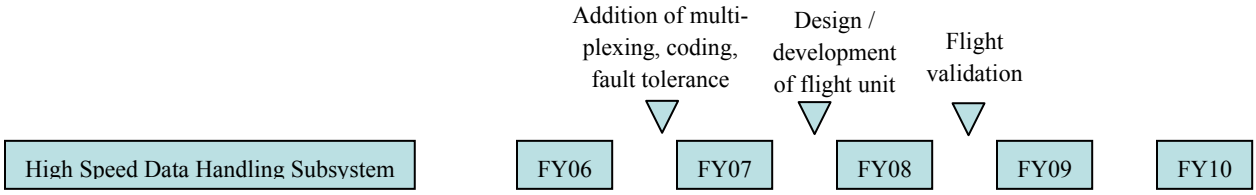
Continued Development

This HSDH Subsystem was originally designed with the Jupiter Icy Moon Orbiter as the target mission. FY06 development work includes the frame multiplexer, Advanced Orbiting Systems (AOS) link layer protocol, Deep Space link coding, additional radio interfaces, and the implementation of newly-developed FPGA fault-tolerance techniques. An FY07 goal is to develop a flight-qualified model and perform a validation flight in FY08.

An early design decision was made to carefully layer the firmware code so that it could be easily adapted to different spacecraft and communication system architectures. As an example, in some systems the solid-state recorder is a separate subsystem and the radios are separate components, so this FPGA implementation of the CFDP/Coding/Link protocol stack would go into a separate telecom support board. In another system, this FPGA could be incorporated as part of a solid-state recorder subsystem that would communicate with external radios. And, in future lunar communication systems, the "Common Communication Software Defined Radio" might incor-

porate both mass memory and the FPGA as part of the radio. See Section 3.7 for further reading and references.

2.7.2 SCHEDULE



2.7.3 POC

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